Filing Date: January 7, 2002

Title: THINNED DIE INTEGRATED CIRCUIT PACKAGE

Assignee: Intel Corporation

REMARKS

Page 7

Dkt: 884.793US1 (INTEL)

Applicant has carefully reviewed and considered the Office Action mailed on August 22, 2003, and the references cited therewith.

Claims 13-27 and 29-44 are now pending in this application.

§102 Rejection of the Claims

Claims 13-27 and 29-44 were rejected under 35 USC § 102(b) as being anticipated by Dawson et al. (U.S. 5,621,615). Applicant respectfully traverses this rejection and requests the Office to consider the following.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." (*Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987), M.P.E.P. §2131, 8th Ed., Rev. 1).

Claim 13 requires "mounting a thinned semiconductor die on a planar surface of a heat spreader." The Office Action asserts "Dawson discloses a method of fabricating an integrated circuit package, comprising mounting a thinned semiconductor die etc." This is incorrect. Dawson neither teaches nor suggests his die is a thinned die. Consequently, Dawson neither expressly nor inherently describes the limitation of claim 13. Because Dawson does not anticipate claim 13, withdrawal of the rejection is respectfully requested.

Applicant notes that since claims 14-15 and 17-23 depend from claim 13, they are likewise not anticipated by Dawson. Withdrawal of the rejection is respectfully requested.

At page 3 the Office Action refers to claim 24, that "Dawson discloses a method of fabricating an integrated circuit package, comprising providing a planar heat spreader; mounting a plurality of thinned semiconductor dice 316, 318 etc." This is incorrect for at least two reasons. First as set forth above, Dawson neither teaches nor suggests his die is a thinned die. Second, Dawson's reference numeral 318 is incorrectly called a die at column 6, lines 27 and 28. But item 318 if first referred to thusly: "The integrated circuit chip 316 has a first major surface 318 and a second major surface 320" (Dawson at column 4, line 1, et seq). Accordingly,

RESPONSE UNDER 37 CFR § 1.111

Serial Number: 10/036389

Filing Date: January 7, 2002

Title: THINNED DIE INTEGRATED CIRCUIT PACKAGE

Assignee: Intel Corporation

Dawson's second reference to item 318 is in error, as it the lead line that points to the chip 316. Any further reference to a plurality of conjoined microelectronic packages is also in error. Withdrawal of the rejection is respectfully requested.

Page 8

Dkt: 884.793US1 (INTEL)

At page 3, the Office Action refers to claim 32, that "Dawson discloses a method of fabricating an integrated circuit package, comprising mounting a thinned semiconductor die on a planar surface of a heat spreader, wherein the thinned semiconductor die has a thickness of no more than 100 μ m etc." This is not correct. The only reference to a thickness is the "die attach thickness [is] in the range of 1.0 mil \pm 60%" (Dawson at column 6, lines 61-62). Accordingly, there is no reference in Dawson to a die thickness and the claims are not anticipated. Withdrawal of the rejection is respectfully requested.

Filing Date: January 7, 2002

Title: THINNED DIE INTEGRATED CIRCUIT PACKAGE

Assignee: Intel Corporation

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney, John Greaves at (801) 278-9171, or the below signed attorney to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743

Respectfully submitted,

CHENG-YI LIU ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. P.O. Box 2938
Minneapolis, Minnesota 55402

Page 9

Dkt: 884.793US1 (INTEL)

(612) 349-9592

Date	Oct.	22	2003

Ann M. McCrackin Reg. No. 42,858

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 22nd day of October, 2003.

Anne M. Richards

Mul

Name Signature